CLAIMS

What is claimed is:

1. An electronic device comprising:

a controller programmed to produce first address data on an output thereof;

a plurality of integrated circuits (ICs) addressable by the controller; and

a shared bus joining the controller and the plurality of ICs;

wherein each of the ICs comprises an input for receiving address data representing an address of the IC on the shared bus, and an output for providing incremented address data, and

wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration.

2. The electronic device claimed in claim 1, wherein each of the ICs further comprises a processor programmed to receive address data at the input, store the address data as the address of the IC, increment the address data, and provide the incremented address data at the output.

3. The electronic device claimed in claim 1, wherein each of the ICs further comprises an address register for storing address data received at its input, and output generator logic for incrementing the address data.

4. The electronic device claimed in claim 1, wherein each of the ICs further comprises means for receiving address data at the input, storing the address data as the address of the IC, incrementing the address data, and providing the incremented address data at the output.

5. The electronic device claimed in claim 1, wherein the address data comprises a binary word.

6. The electronic device claimed in claim 1, wherein the address data comprises a series of pulses representing an address value.

7. The electronic device claimed in claim 1, further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce first address data on the output thereof.

8. An electronic device comprising:

means for generating first address data at an output of a controller;

means for receiving the first address data at an input of a first IC;

means for storing the first address data in the first IC as an address of the first IC;

means for incrementing the first address data in the first IC to produce first incremented address data; and

means for providing the first incremented address data to a second IC through an output of the first IC.

9. A method for initializing addresses of a plurality of integrated circuits, comprising:

generating first address data at an output of a controller;

receiving the first address data at an input of a first IC;

storing the first address data in an address register of the first IC;

incrementing the first address data in the first IC to produce first incremented address data; and

providing the first incremented address data to a second IC through an output of the first IC.

10. The method for initializing claimed in claim 9, further comprising:

receiving the first incremented address data at an input of a second IC;

storing the first incremented address data in an address register of the second IC;

incrementing the first incremented address data in the second IC to produce second incremented address data; and

providing the second incremented address data at an output of the second IC.

11. An electronic device comprising:

a controller;

a plurality of integrated circuits (ICs) addressable by the controller; and

a shared bus joining the controller and the plurality of integrated circuits;

wherein the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses,

wherein each of the ICs comprises an input for receiving an enable signal and an output for providing an enable signal in conjunction with a change in address data on the shared bus, and means for storing an address present on the shared bus as an address of the IC in response to receiving an enable signal, and

wherein the input of a first IC communicates with the output of the controller and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration.

12. The electronic device claimed in claim 11, wherein each of said ICs further comprises a first logic circuit for storing an address present on the shared bus as an address of the IC upon receipt of an enable signal.

13. The electronic device claimed in claim 12, wherein each of said ICs further comprises a second logic circuit for generating an enable signal in conjunction with a change in address data on the shared bus.

14. The electronic device claimed in claim 13, wherein said second logic circuit comprises a timer that is initialized upon receipt of an input enable signal, and that generates an output enable signal after a period of time that coincides with a rate of address data on the shared bus.

15. The electronic device claimed in claim 13, wherein said second logic circuit produces an output enable signal upon detecting a first change in address data on the shared bus after receiving an input enable signal.

16. The electronic device claimed in claim 11, wherein each of said ICs comprises a processor programmed to initialize a timer upon receipt of an enable signal, and generate an enable signal upon expiration of the timer.

17. The electronic device claimed in claim 11, wherein each of said ICs comprises a processor programmed to receive an enable signal at the input, store address data present on the shared bus as the address of the IC in response to the enable signal, detect a change in the address data on the shared bus, and generate an enable signal at the output in response to the change in the address data.

18. The electronic device claimed in claim 11, wherein each of said ICs comprises:

means for receiving an enable signal at the input; and

means for generating an enable signal at the output in conjunction with the change in the address data.

19. The electronic device claimed in claim 11, further comprising a storage medium in communication with the controller and having stored therein programming instructions for instructing the controller to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses.

20. An electronic device comprising:

means for generating an enable signal at an output of a controller and generating first address data on a shared bus;

means for receiving the enable signal generated at the output of the controller at an input of a first IC;

means for receiving the first address data at a shared bus input of the first IC;

means for storing the first address data in an address register of the first IC upon coincidence of the enable signal and the first address data; and

means for providing an enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus.

21. A method for initializing addresses of a plurality of integrated circuits, comprising:

generating an enable signal at an output of a controller and generating first address data on a shared bus;

receiving the enable signal generated at the output of the controller at an input of a first IC;

receiving the first address data at a shared bus input of the first IC;

storing the first address data in an address register of the first IC upon coincidence of the enable signal and the first address data; and

providing an enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus.

22. A method as claimed in claim 19, further comprising:

receiving the enable signal provided at the output of the first IC at the input of a second IC;

storing a second address data present on the shared bus in an address register of the second IC; and

generating an enable signal at an output of the second IC in conjunction with a change in address data present on the shared bus.

23. The method claimed in claim 21, wherein generating the enable signal at the output of the first IC comprises initializing a timer upon receipt of the enable signal at the input of the first IC, and generating the enable signal at the output upon expiration of the timer.

24. The method claimed in claim 21, wherein the enable signal is generated at the output of the first IC upon detection of a change in address data after receiving an enable signal at the input of the first IC.